* K C - 6 2 2 7 *

# KC-6227

## B. E. - II (Sem. III) (IC) Examination

### November / December – 2012

## Digital Circuits

Time : **3** Hours] [Total Marks : **100**

**Instructions :**

(1)

નીચે દર્શાવેલ ☛ નિશાનીવાળી વિગતો ઉત્તરવહી પર અવશ્ય લખવી.
**Fillup strictly the details of ☛ signs on your answer book.**

Name of the Examination :

☛ B. E. - 2 (SEM. 3) (IC)

Name of the Subject :

☛ DIGITAL CIRCUITS

☛ Subject Code No. : 6 2 2 7 ☛ Section No. (1, 2,.....) : NIL

Seat No. :

Student's Signature

(2) Attempt all questions.

(3) Assume suitable data wherever required.

(4) Figures to the right indicate full marks.

**1** (a) Answer the following questions : **10**

(1) Draw the symbol and truth table of Ex- NOR gate

(2) Implement AND gate using NAND gates only.

(3) Simplification of (A + B) (A + B') is _____.

(4) _____ is the binary equivalent of Octal number (123).

(5) _____and _____ are called universal gates.

(6) What is the dual of A + AB + ABC = A.

(7) _____ is the gray code of 110011.

(8) 1's complement of 11100011 is _____.

(9) What is the full form of ASCII ?

(10) What is the 9's complement of decimal number 345 ?

(b) Explain 3 to 8 line decoder with truth table and circuit diagram. **6**

(c) Realize Ex-NOR gate with NAND gates only. **4**

**2** (a) Explain Full adder circuit diagram and truth table. **8**

(b) Simplify following boolean functions using K-map and implement using logic gates : **7**

$F(a,b,c,d) = \Sigma m\ (1,5,7,9,11,13,15)$

**OR**

**2** (a) Design a combinational logic circuit whose out put is high only when 4 bit input is divisible by three. **8**

(b) Simplify the following Boolean function using tabulation method : **7**

$F(A,B,C,D) = \Sigma m(0,1,3,7,8,9,11,15)$

**3** Attempt any **three** : **15**

(1) Explain BCD adder circuit.

(2) Construct 5 × 32 line decoder with the help of four 3 × 8 line decoder and one 2 × 4 line decoder.

(3) Design 3 bit even parity generator and checker circuit.

(4) Implement following boolean function using 8 : 1 multiplexer :

$F(A, B, C, D) = \Sigma m(1, 2, 4, 5, 7, 9, 14)$

(5) Design binary to gray code converter circuit.

**4** (a) Attempt any **five** : **10**

(1) What do you mean by Race around condition?

(2) What do you mean by the edge trigger filp-flop ?

(3) List Types of Shift Register.

(4) Draw circuit to convert JK Flipflop to T Flipflop.

(5) Differentiate Synchronous and asynchronous circuits.

(6) Draw block diagram of the sequential circuit.

(7) The number of flipflop required to implement mod-10 counter are _____.

(b) Draw and Explain JK flipflop with NAND Gates. **10**

**5** Attempt any **two** : **16**

(a) Explain Bidirectional Shift register in detail.

(b) Explain ROM in detail.

(c) Draw SR Latch circuit with Truth table Excitation table and Char. Equation.

**6** Attempt any **two** : **14**

(a) Convert SR flipflop to JK Flipflop.

(b) Convert JK Flipflop to SR Flipflop.

(c) Explain Application of Flipflops in detail.